WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a non-conductive film defining opposed top and bottom film surfaces and including a plurality of openings disposed therein;

a die pad defining opposed top and bottom die pad surfaces, the top die pad surface being attached to the bottom film surface such that at least a portion of the top die pad surface is exposed within one of the openings;

a plurality of leads defining opposed top and bottom lead surfaces, the top lead surface of each of the leads being attached to the bottom film surface such that at least a portion of the top lead surface of each of the leads is exposed within a respective one of the openings;

a semiconductor die attached to the exposed portion of the top die pad surface and electrically connected to the exposed portion of the top lead surface of at least one of the leads; and

a package body at least partially covering the semiconductor die, the film, the die pad and the leads such that the bottom die pad surface, the bottom lead surface of each of the leads, and at least portions of the bottom film surface are exposed in the package body.

2. The semiconductor package of Claim 1 wherein the leads are arranged in a first row which circumvents the die pad in spaced relation thereto, and a second row which circumvents the first row.

3. The semiconductor package of Claim 2 wherein the leads of the second row are staggered relative to the leads of the first row.

4. The semiconductor package of Claim 2 further comprising at least one ring circumventing the die pad and extending between the die pad and the leads of the first row.

5. The semiconductor package of Claim 1 wherein the bottom lead surface of each of the leads has a quadrangular configuration.

6. The semiconductor package of Claim 1 wherein the exposed portion of the top lead surface of each of the leads has an immersion gold layer formed thereon.

7. The semiconductor package of Claim 6 wherein the semiconductor die is electrically connected to the exposed portion of the top lead surface of each of the leads by a respective one of a plurality of bond wires.

8. The semiconductor package of Claim 1 wherein the top and bottom film surfaces, the top and bottom die pad surfaces, and the top and bottom lead surfaces of each of the leads are generally planar.

9. A semiconductor package, comprising:

a non-conductive film defining opposed top and bottom film surfaces and including a plurality of openings disposed therein;

a die pad defining opposed top and bottom die pad surfaces, the bottom die pad surface being attached to the top film surface such that at least a portion of the bottom die pad surface is exposed within one of the openings;

a plurality of leads defining opposed top and bottom lead surfaces, the bottom lead surface of each of the leads being attached to the top film surface such that at least a portion of the bottom lead surface of each of the leads is exposed within a respective one of the openings;

a semiconductor die attached to the top die pad surface and electrically connected to the top lead surface of at least one of the leads; and

a package body at least partially covering the semiconductor die, the film, the die pad and the leads such that the bottom film surface and at least portions of the bottom die pad surface and the bottom lead surface of each of the leads are exposed in the package body.

10. The semiconductor package of Claim 9 further comprising solder bumps applied to each of the exposed portions of the bottom lead surfaces and to the exposed portion of the bottom die pad surface, the solder bumps protruding beyond the bottom film surface.

11. The semiconductor package of Claim 9 wherein the leads are arranged in a first row which circumvents the die pad in spaced relation thereto, and a second row which circumvents the first row.

12. The semiconductor package of Claim 11 wherein the leads of the second row are offset relative to the leads of the first row.

13. The semiconductor package of Claim 11 further comprising at least one ring circumventing the die pad and extending between the die pad and the leads of the first row.

14. The semiconductor package of Claim 9 wherein the exposed portion of the bottom lead surface of each of the leads has a quadrangular configuration.

15. The semiconductor package of Claim 9 wherein the top lead surface of each of the leads has an immersion gold layer formed thereon.

16. The semiconductor package of Claim 15 wherein the semiconductor die is electrically connected to the top lead surface of each of the leads by a respective one of a plurality of bond wires.

17. The semiconductor package of Claim 9 wherein the top and bottom film surfaces, the top and bottom die pad surfaces, and the top and bottom lead surfaces are each generally planar.

18. A semiconductor package, comprising:

a non-conductive film having a plurality of openings disposed therein;

a die pad attached to the film such that at least a portion of the die pad is exposed within one of the openings;

a plurality of leads attached to the film and arranged in at least inner and outer rows which each circumvent the die pad, at least a portion of each of the leads being exposed in a respective one of the openings;

a semiconductor die attached to the die pad and electrically connected to at least one of the leads; and

a package body at least partially covering the semiconductor die, the film, the die pad, and the leads such that portions of the die pad and the leads are exposed in a common surface of the package body.

19. The semiconductor package of Claim 18 further comprising at least one ring disposed between the die pad and the inner row of the leads.

20. The semiconductor package of Claim 18 wherein the leads of the outer row are staggered relative to the leads of the inner row.